IN THE DRAWINGS

Please amend Figs. 1 and 2 as indicated on the enclosed copies thereof. Fig. 1 has been amended to include the reference characters "10" and "21," and the element "USB LINK layer" indicated therein to include the reference numeral "16." Fig. 2 has been amended to correct the description of the reference character 49 to read "BIST comparator."

REMARKS

I. Introduction

Applicants and Applicants' representative would like to thank Examiner Zheng for the indication allowance of claims 17-22, and for the indication of allowable subject matter recited by claim 4, 6-8 and 11-16. In response to the Office Action dated December 30, 2004, Applicants have amended Fig. 1 so as to include the reference characters "10" and "21," and the element "USB LINK layer" indicated therein to include the reference numeral "16," and Fig. 2 to correct the description of the reference character 49 to read "BIST comparator." The Specification and the Abstract have also been amended so as to address the pending objections. Also, Applicants have rewritten claims 4 and 6 into independent format. Additionally, claims 1 and 23 are amended so as to further clarify the claimed invention. Claims 26 and 27 are added. Support for these amendments can be found, for example, in Fig. 2, and its corresponding section of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. Telephonic Interview

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Zheng. Applicant and Applicant's representative would like to thank Examiner Zheng for her courtesy in conducting the interview on March 18, 2005 and for her assistance in resolving issues. During the interview, Applicants' representative explained that it appears that the Examiner has made a procedural error with respect to the rejection of claim 1. In particular, the Examiner has indicated that claim 11 contains allowable subject matter in the

pending Office Action. Upon review, it is noted that claim 1 also recites this claimed limitation, which should have rendered claim 1 allowable. As a result of the interview, the Examiner has concluded that claim 9 should have been rejected, but tentatively agreed to consider the enclosed amendment to independent claims 1 and 23, which is submitted to place the application in clear and immediate condition for allowance for the reasons set forth below. The Examiner has also agreed that the next Office Action will be issued as a ***non-final*** Office Action so as to correct the aforementioned error.

III. The Rejection Of Claims 1-3, 5 and 23-25 Under 35 U.S.C. § 102

Claims 1-3, 5 and 23-25 are rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 6,298,458 to Cranford. Applicants respectfully request reconsideration of this rejection for the reasons set forth below.

Claim 1, as amended, recites in-part a first signal is input to said self-test data generator and a second signal is input to said test data analyzer so that one of said self-test data generator and said test data analyzer is capable of being activated or deactivated without activating or deactivating the other.

In accordance with one exemplary embodiment of the present invention, the TX-BIST circuit 35 is enabled by activating the TX-BIST enable signal, while the BIST analyzer circuit 49 is enabled by activating the RX-BIST enable signal. For example, by disabling the TX-BIST enable signal (thereby turning off the TX-BIST circuit 35), data can be input directly into the multiplexer 36 in the self-test mode via the bus 21. In addition, the very same data can be input into the BIST analyzer circuit 49 via the bus 21. Consequently, the self-test can be performed on the external data input to the multiplexer 36, which is then transmitted by the transmitter section

31 to the receiver section 32, and subsequently verified by the BIST analyzer circuit 49 in the same manner as the TX-BIST circuit 35. Accordingly, if an error is found, the TX-BIST circuit 35 can be isolated while all other circuits are verified by the self-test. As a result, the present invention advantageously activates or deactivates one of the TX-BIST circuit 35 and the BIST analyzer circuit 49 without having to activate or deactivate the other circuit so as to accurately and expeditiously detect any possible error in the transmitter or receiver section that would otherwise be undetectable.

In direct contrast, the transmit BIST 175 or the receive BIST 205 of Cranford is incapable of being activated or deactivated without activating or deactivating the other. As illustrated in Fig. 4 of Cranford, a sequential data bitstream or a BIST signal 221 is generated by the transmit BIST 175 for input to the analog transmitter 125. In response, a periodic data signal 213 is broadcast from the analog transmitter 125 for receipt by the analog receiver 150. Particularly, the bi-directional bus 202 ***enables*** the receive BIST 205 to receive the data ***transmitted by the transmit 175*** from the receiver 150 so as to activate the counter systems 222/226/228/232 therein (see, e.g., col. 5, lines 20-42 and col. 6, lines 36-50). Accordingly, it is respectfully submitted that such a conventional BIST circuit does ***not*** allow one of the transmit BIST 175 and the receive BIST 205 to be enabled while the other is disabled. Indeed, if the transmit BIST 175 is disabled, it appears that the ***entire*** transceiver including the receive BIST 205 will be disabled.

Furthermore, it is also noted in the rejection to claim 2, col. 4, lines 60-62 and 219/220/223 are relied upon as allegedly disclosing an "enabling-disabling" feature. However, at the cited portion, the receive BIST 205 merely asserts additional control over the protocol generation so as to disable the scrambling methodologies present in the conventional transceiver,

which is ***irrelevant*** and unrelated to determining the condition of the transmit BIST 175, let alone disclose disabling the transmit BIST 175 while the receive BIST 205 is enabled.

For all of these reasons, it is respectfully submitted that Cranford is silent with regard to having any capability to activate or deactivate the transmit BIST 175 or the receive BIST 205 without activating or deactivating the other. Thus, Cranford does not disclose or suggest the claim limitation recited by claim 1.

With respect to claim 23, as this claim also includes the feature "wherein a first signal is input to said self-test data generator and a second signal is input to said test data analyzer so that one of said self-test data generator and said test data analyzer is capable of being activated or deactivated without activating or deactivating the other," it is respectfully submitted that claim 23 is allowable for reasons similar to those discussed above with respect to claim 1.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Cranford fails to disclose or suggest the foregoing claim elements, it is clear that Cranford does not anticipate claim 1 or 23, or any of the claims dependent thereon.

IV. The Rejection Of Claims 9 and 10 Under 35 U.S.C. § 103

Claims 9-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 6,201,829 to Schneider. Applicants respectfully traverse the rejection for at least the following reasons.

Claim 9 recites in-part, "... test data analyzer comprising a ***second pseudo-random number generator*** ... having a programmable data value, said data value being input into said second pseudo random number generator via an external bus ***coupled*** to said test data analyzer.

In the pending rejection, the Examiner relies on Fig. 5 and col. 8, line 60 to col. 9, line 6 as allegedly disclosing a second pseudo-random number generator. The Examiner admits that Schneider does not disclose that the data value is input via an external bus coupled to the self-test data generator, but nonetheless maintains the rejection because "it is well known that there are many bus lines going through the pseudo-random generator and data."

However, it is respectfully submitted that this statement as a prelude to the rejection is not a proper basis for rejecting Applicants' claims, as the statement is directed to the ***Examiner's opinion*** rather than what is taught by the prior art. It is submitted that the "Examiner's opinion" cannot be relied on to replace the deficiency of a prior art reference. If the pending rejection intended to take Official Notice that the differences between Schneider and the present invention as recited in the rejected claims are well-known in the art, then pursuant to **M.P.E.P. § 2144.03**, Applicants respectfully traverse such an assertion and request the Examiner to cite one or more references in support of this position (see, second paragraph, last three lines of **M.P.E.P. § 2144.03**).

Even assuming *arguendo* that the Examiner's opinion is proper, claim 9 does not merely recite an external bus. Rather, claim 9 also recites "...data value being ***input into*** the second random number generator via an external bus ***coupled to*** said test data analyzer." In other words, claim 9 requires the external bus to provide communication between the second random number generator and the test data analyzer. With regard to the Examiner's statement that pseudo-random generators are generally connected to the bus lines, Applicants do not dispute this

conclusion. However, the prior art does not discuss or even recognize the ***specific*** bus connection as recited by the pending claims. Specifically, the rejection has not provided any requisite objective evidence ***from the cited prior art*** in supporting the argument that the alleged second pseudo-random number generator ***necessarily*** receives a programmable data value ***from*** the alleged test data analyzer, let alone doing so via an external bus. Absent this teaching, it is respectfully submitted that the proposed modification is based solely on improper hindsight reasoning, whereby the pending rejection has selected bits and pieces of the claimed invention from plural references and used only Applicants' specification as a guide to reconstruct the claimed invention. By contrast, the data bus 21 of the present invention is connected to the input port of the pseudo-random number generator circuit 65, such that when the "load-enable" signal is enabled, the data word on the data bus 21 is read into the random number generator 65 via the BIST analyzer circuit 49 (see, e.g., page 16, lines 3-15 of the specification). Therefore, for at least these reasons, the proposed modification fails to establish *prima facie* obviousness of the pending claims.

Furthermore, it would appear that the pending rejection merely ***assumes*** that the BIST signature analyzer 61 of Schneider includes the alleged second pseudo-random number generator without providing or identifying any support for the allegation. However, without any basis or rationale presented in support of this assertion, it is difficult for the Applicants to understand the basis of these rejections and to provide a proper rebuttal. As best understood, the rejection assumes that because the alleged self-test data generator 62 of Schneider is a pseudo-random built-in self test pattern generator, the alleged test data analyzer 61 may also perceivably operate as a pseudo-random test data analyzer so as to inherently include a pseudo-random number generator to arrive at the claimed invention. However, this inaccurate analysis completely

ignores the fact that the signature analyzer 61 is utilized ***only*** to ***evaluate*** the signal pattern provided on the receiver bus 36 against the data mask pattern identical to the final pattern generated by the BIST circuit 62. Specifically, if a match is found therebetween, then the signature analyzer 61 ***asserts*** a qualification signal in response to such a match. In other words, the signature analyzer 61 merely ***compares*** the pattern transmitted by the BIST circuit 62 and that processed by the receiver, and does not generate any pseudo-random number in the manner alleged by the Examiner. Indeed, Schneider is silent with regard to a second pseudo-random number, let alone disclose doing so via a second pseudo-random number generator coupled to the alleged test data analyzer. At best, Schneider has arguably shown a BIST transceiver without demonstrating its receiving portion as having a pseudo-random number generator, let alone disclose supplying a programmable data value thereto. Therefore, it is respectfully submitted that Schneider is no more relevant to the present invention than Applicants' admitted prior art.

Indeed, as described at pages 1-2 of the specification, in order to accurately evaluate the functionally of a transceiver, the transceiver is typically tested under normal operating conditions by using the conventional BIST circuit. Specifically, the data routed through the transmitter section is also routed to the receiver section of the transceiver. Upon being processed by the receiver section, the received data is ***compared*** with that generated by the transmitter section. If a match is found therebetween, the transceiver is then confirmed to operate correctly. However, the instant inventors have discovered that the conventional BIST circuit for testing the transceivers do not provide any means for controlling and/or varying the input data during the testing process. The Applicants have further found that the conventional BIST circuit does not control the transmitter section and the receiver section separately during the self-test process. As such, a complete test using varying data can not be expressly performed, and any component

failure of the transceiver cannot be readily identified and isolated. Accordingly, by implementing a BIST circuit having a self-test data generator and a test data analyzer that are separately and independently controlled, the transceiver of the present invention advantageously provides the necessary data variation for testing all protocols of data transmission, and expeditiously detects errors in the transmitter or receiver section that would otherwise be undetectable.

In this regard, Schneider, at best, is merely cumulative to the admitted prior art described at pages 1-3 of Applicants' specification in that Schneider is also subject to the same drawbacks as those of the admitted prior art resulting from the inability to detect errors in the transmitter section or the receiver section separately, identified by the instant inventors at pages 2-3 of Applicants' specification. Only Applicants have recognized and considered the problems associated with the conventional BIST circuits, and provided the means by which to overcome such problems.

Thus, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and Schneider fails to do so, it is respectfully submitted that claim 9 is patentable over the cited prior art.

V. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,*

819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 1, 9 and 23 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

VI. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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